Paragraph numbered 0011:

The gate 126 of the GGNMOS transistor 105 separates the first and second N+ regions 112 and 110. Furthermore, the GGNMOS transistor 105 is used to "trigger", i.e., turn on the SCR. In particular, the GGNMOS transistor 105 is an N-channel MOS transistor, which includes a drain 129 and source 127, which are respectively formed by the second N+ region 110 and the first N+ region 112. The NMOS-channel is formed at the surface of the P-well region 120 between the first and second N+ regions 112 and 110. Additionally, since the gate 126 is grounded, the P-well region 120 is prevented from forming the NMOS-channel between the first and second N+ regions 112 and 110, thereby preserving the functionality of the SCR's bipolar transistor T1 131.

Paragraph numbered 0018:

As such, once the NPN transistor T1 131 is turned on, the T1 131 collector provides the base current to the PNP transistor T2 132. Therefore, the base current of the PNP transistor T2 132 is greater than the base current of the NPN transistor T1 131. Moreover, the current gain β_2 of the PNP transistor T2 132 is realized as the T2 132 collector current, which is then fed back to the base of the NPN transistor T1 131, thereby amplifying the base current of the NPN transistor T1 131. This amplification of the base currents in the SCR 102 progressively continues to increase in a loop between both transistors T1 131 and T2 132. Therefore, the conduction occurring in a turned on SCR is also called a "regenerative process".

Paragraph numbered 0040:

The coupled trigger NMOS transistor 206 (as shown in the schematics of FIG. 2A) allows the SCR 202 to turn on faster than the prior art LVTSCR device (see FIG 1A). Specifically, the drain of the NMOS transistor 206 is no longer coupled to the collector of the NPN transistor T1 231 (also, base of the PNP transistor T2 232), which was used to provide a reverse biased breakdown voltage between the N^+ region 110 (base) of the PNP transistor T2 232 and the P-well region 120 (base) of the NPN transistor T1 231. Rather, the drain is coupled to the pad 148, while the source and the

gate of the NMOS transistor 206 are coupled directly to the base of the NPN transistor T1 231, which is discussed below in detail with regard to FIGS. 3 and 4.

Paragraph numbered 0041:

Furthermore, a person skilled in the art for which this invention pertains will understand that a PMOS triggered SCR ESD protection device may also be utilized. For example, FIG. 2B depicts an illustrative schematic diagram E representing a PMOS triggered SCR ESD protection device 201 of the present invention. Furthermore, a person skilled in the art will recognize that a PMOS transistor with drain-bulk-gate coupling, or two cascoded PMOS transistors, or other external triggering devices 205 may used as part of ESD protection device 201, as discussed above. For purposes of clarity, the invention will be discussed as a NMOS triggered SCR as illustratively depicted in the schematic diagram A of FIG. 2A.

Delete paragraph numbered 0042.

Paragraph numbered 0043:

FIG. 3 depicts a cross-sectional view of a SCR 202 of the NMOS-triggered SCR ESD protection device 201 of FIGS. 2A and 2B. Specifically, the protection device 201 includes in part, a P-type substrate 303, into which an N-well 304 and P-well 306 is formed. The N-well 304 and P-well 306 are adjacent to each other and form a junction 307 at the adjoining boundary. Within the N-well 304, a first P+ region 308 is formed. Furthermore, within the P-well 306, a single N+ region 312 and a second P+ region 314 are formed thereupon. The regions denoted P+ and N+ are regions having higher doping levels than the N-well and P-well regions 304 and 306. Furthermore, it should be noted that there is no "second N+ region 110" formed over and overlapping the junction 307 between both the P-well 304 and N-well 306 regions, as shown in the prior art of FIG. 1B.

IN THE CLAIMS

Please replace claims 2, 4, 15, 17, and 24 as rewritten below: